



# FXM2IC102

## Dual Supply 2-Bit I<sup>2</sup>C Interface Voltage Translator with Configurable Voltage Supplies and Signal Levels and Auto Direction Sensing

### Features

- Bi-directional interface between any two levels from 1.65V to 5.5V
- Buffer isolates capacitance and allows 400pF on each port
- Open-drain inputs/outputs
- Accommodates Standard-mode and Fast-mode I<sup>2</sup>C-bus devices
- Fully configurable: Inputs and outputs track V<sub>CC</sub> level
- Non-preferential power-up; either V<sub>CC</sub> may be powered-up first
- Outputs remain in 3-state until active V<sub>CC</sub> level is reached
- Outputs switch to 3-state if either V<sub>CC</sub> is at GND
- Power off high impedance
- Active high output enable referenced to V<sub>CCA</sub> voltage
- 5V tolerant output enable
- Packaged in 8-terminal leadless MicroPak (1.6mm x 1.6mm)
- Direction control not needed
- ESD protection exceeds:
  - 8kV HBM ESD (per JESD22-A114 & Mil Std 883e 3015.7)
  - 15kV HBM I/O to GND ESD (per JESD22-A114 & Mil Std 883e 3015.7)

### General Description

The FXM2IC102 is a configurable dual-voltage-supply translator designed for bi-directional voltage translation over a wide range of input and output voltages levels.

The FXM2IC102 is intended for use as a voltage translator in applications using the I<sup>2</sup>C bus interface. Input and output voltage levels are compatible with I<sup>2</sup>C device specification voltage levels.


The device is designed so that the A port tracks the V<sub>CCA</sub> level, and the B port tracks the V<sub>CCB</sub> level. This allows for bi-directional voltage translation over the voltage ranges: 1.8V, 2.5V, 3.3V, 5.0V.

The device remains in 3-state until both V<sub>CC</sub>s reach active levels allowing either V<sub>CC</sub> to be powered-up first. Internal power down control circuits place the device in 3-state if either V<sub>CC</sub> is removed.

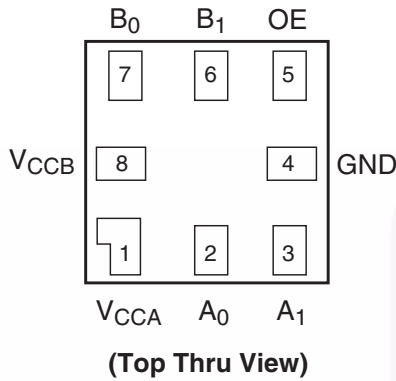
The two ports of the device have auto-direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

### Ordering Information

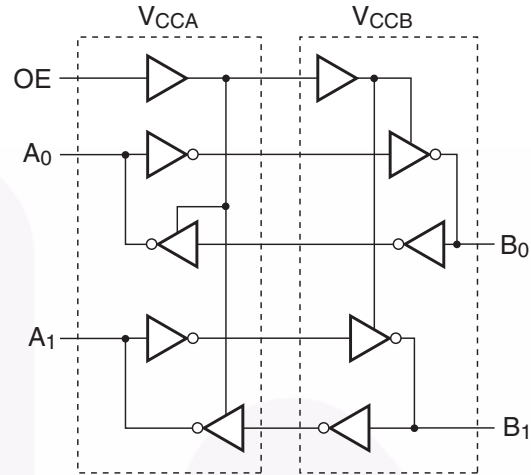
Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
FXM2IC102L8X	MAC08A	XG	8-Lead MicroPak, 1.6 mm Wide	3k Units on Tape and Reel

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



### Functional Diagram



### Pin Description

Number	Name	Description
1	V <sub>CCA</sub>	A Side Power Supply
2, 3	A <sub>0</sub> , A <sub>1</sub>	A Side Inputs or 3-State Outputs
4	GND	
5	OE	Output Enable Input
6, 7	B <sub>1</sub> , B <sub>0</sub>	B Side Inputs or 3-State Outputs
8	V <sub>CCB</sub>	B Side Power Supply

### Function Table

Control	Outputs
OE	
L	3-State
H	Normal Operation

H = HIGH Logic Level

L = LOW Logic Level

### Power-Up/Power-Down Sequencing

FXM translators offer an advantage in that either V<sub>CC</sub> may be powered up first. This benefit derives from the chip design. When either V<sub>CC</sub> is at 0V, outputs are in a high-impedance state. The control input (OE) is designed to track the V<sub>CCA</sub> supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is the following:

1. Apply power to the first V<sub>CC</sub>.
2. Apply power to the second V<sub>CC</sub>.
3. Drive the OE input high to enable the device.

The recommended power-down sequence is the following:

1. Drive OE input low to disable the device.
2. Remove power from either V<sub>CC</sub>.
3. Remove power from other V<sub>CC</sub>.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CCA}, V_{CCB}$	Supply Voltage	-0.5V to +7.0V
$V_I$	DC Input Voltage A Port B Port Control Input (OE)	-0.5V to +7.0V -0.5V to +7.0V -0.5V to +7.0V
$V_O$	Output Voltage <sup>(1)</sup> $A_n$ Outputs 3-State $B_n$ Outputs 3-State $A_n$ Outputs Active $B_n$ Outputs Active	-0.5V to +7.0V -0.5V to +7.0V -0.5V to $V_{CCA} + 0.5V$ -0.5V to $V_{CCB} + 0.5V$
$I_{IK}$	DC Input Diode Current @ $V_I < 0V$	-50mA
$I_{OK}$	DC Output Diode Current @ $V_O < 0V$ $V_O > V_{CC}$	-50mA +50mA
$I_{OH} / I_{OL}$	DC Output Source/Sink Current	-50mA / +50mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin	±100mA
$T_{STG}$	Storage Temperature Range	-65°C to +150°C

**Note:**

1.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(2)</sup>

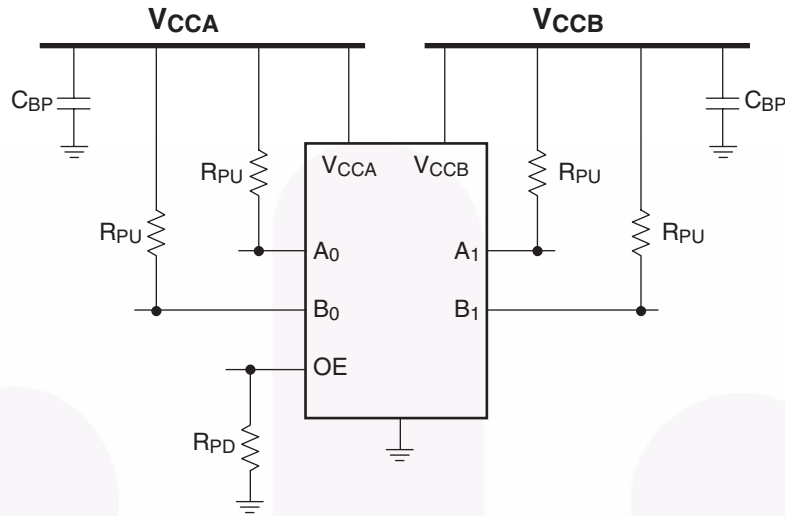
The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CCA}$ or $V_{CCB}$	Power Supply Operating	1.65V to 5.5V
$V_I$	Input Voltage A Port B Port Control Input (OE)	0.0V to 5.5V 0.0V to 5.5V 0.0V to $V_{CCA}$
$\Delta t / \Delta v$	Maximum Input Edge Rate $V_{CCA/B} = 1.65V$ to 5.5V	200ns/V
$T_A$	Free Air Operating Temperature	-40°C to +85°C

**Note:**

2. All unused inputs and I/O pins must be held at  $V_{CCI}$  or GND.

## FXM2IC102 Application Circuit



### Application Notes

The FXM2IC102 has open-drain outputs and requires pull-up resistors on the four data I/O pins as shown in the above figure. If a pair of data I/O pins (A<sub>n</sub>/B<sub>n</sub>) are not used, they both should be tied to Gnd (or both to V<sub>CC</sub>). In this case, pull-down or pull-up resistors are not required.

The recommended values for the pull-up resistors (R<sub>PU</sub>) are 1kΩ minimum to 10kΩ maximum. The recommended value for the bypass capacitors (C<sub>BP</sub>) is 1.1μF. The recommended value for the pull-down resistor (R<sub>PD</sub>) on OE is 1kΩ or higher and may depend upon the current-sinking capability of the device driving the OE pin.

### DC Electrical Characteristics (T<sub>A</sub> = -40°C to +85°C)

Symbol	Parameter	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	Conditions		Min.	Max.	Units
V <sub>IHA</sub>	High Level Input Voltage	1.65–5.5	1.65–5.5	Data Inputs A <sub>n</sub>		0.7 x V <sub>CCA</sub>		V
		1.65–5.5	1.65–5.5	Control Input OE		0.9 x V <sub>CCA</sub>		
V <sub>IHB</sub>		1.65–5.5	1.65–5.5	Data Inputs B <sub>n</sub>		0.7 x V <sub>CCB</sub>		V
V <sub>ILA</sub>	Low Level Input Voltage	1.65–5.5	1.65–5.5	Data Inputs A <sub>n</sub>			0.3 x V <sub>CCA</sub>	V
		1.65–5.5	1.65–5.5	Control Input OE			0.1 x V <sub>CCA</sub>	
V <sub>ILB</sub>		1.65–5.5	1.65–5.5	Data Inputs B <sub>n</sub>			0.3 x V <sub>CCB</sub>	V
V <sub>OLA</sub> <sup>(3)</sup>	Low Level Output Voltage	1.65–2.3	1.65–5.5	A Port	I <sub>OL</sub> = 3mA		0.1 x V <sub>CCA</sub>	V
		3.0–5.5	1.65–5.5		I <sub>OL</sub> = 6mA		0.2	
V <sub>OLB</sub> <sup>(3)</sup>		1.65–5.5	1.65–2.3	B Port	I <sub>OL</sub> = 3mA		0.1 x V <sub>CCB</sub>	V
		1.65–5.5	3.0–5.5		I <sub>OL</sub> = 6mA		0.2	
I <sub>I</sub>	Input Leakage Current	1.65–5.5	1.65–5.5	Control input OE, V <sub>I</sub> = V <sub>CCA</sub> or GND			±1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	0	5.5	A <sub>n</sub>	V <sub>I</sub> or V <sub>O</sub> = 0V to 5.5V		±2.0	μA
		5.5	0	B <sub>n</sub>	V <sub>I</sub> or V <sub>O</sub> = 0V to 5.5V		±2.0	
I <sub>OZ</sub> <sup>(4)</sup>	3-State Output Leakage	5.5	5.5	A <sub>n</sub> , B <sub>n</sub>	V <sub>O</sub> = 0V to 5.5V, OE = V <sub>IL</sub>		±2.0	μA
		5.5	0	A <sub>n</sub>	V <sub>O</sub> = 0V to 5.5V, OE = Don't Care		±2.0	
		0	5.5	B <sub>n</sub>	V <sub>O</sub> = 0V to 5.5V, OE = Don't Care		±2.0	
I <sub>CCA/B</sub> <sup>(5)(6)</sup>	Quiescent Supply Current	1.65–5.5	1.65–5.5	V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0			5.0	μA
I <sub>CCZ</sub> <sup>(5)</sup>	Quiescent Supply Current	1.65–5.5	1.65–5.5	V <sub>I</sub> = V <sub>CC1</sub> or GND, I <sub>O</sub> = 0, OE = V <sub>IL</sub>			5.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	0	1.65–5.5	V <sub>I</sub> = 5.5V or GND, I <sub>O</sub> = 0, OE = Don't Care, B <sub>n</sub> to A <sub>n</sub>			-2.0	μA
		1.65–5.5	0				2.0	
I <sub>CCB</sub>	Quiescent Supply Current	1.65–5.5	0	V <sub>I</sub> = 5.5V or GND, I <sub>O</sub> = 0, OE = Don't Care, A <sub>n</sub> to B <sub>n</sub>			-2.0	μA
		0	1.65–5.5				2.0	

**Notes:**

3. This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”
4. “Don't Care” indicates any valid logic level.
5. V<sub>CC1</sub> is the V<sub>CC</sub> associated with the input side.
6. Reflects current per supply, V<sub>CCA</sub> or V<sub>CCB</sub>.

## Dynamic Output Electrical Characteristics

### Output Rise/Fall Time and Dynamic Output Current<sup>(7)</sup>

Output Load:  $C_L = 50\text{pF}$ ,  $R_L = 1\text{k}\Omega$

Symbol <sup>(8)</sup>	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, V_{CCO} =$								Units
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
$t_{\text{rise}}^{(9)}$	Output Rise Time, A Port, B Port		4.0		5.0		6.0		8.0	ns
$t_{\text{fall}}^{(10)}$	Output Fall Time, A Port, B Port		4.0		5.0		6.0		8.0	ns
$I_{\text{OHD}}^{(9)}$	Dynamic Output Current HIGH	-45		-24		-15		-8.0		mA
$I_{\text{OLD}}^{(10)}$	Dynamic Output Current LOW	+45		+24		+15		+8.0		mA

### Maximum Data Rate<sup>(11)</sup>

Output Load:  $C_L = 50\text{pF}$ ,  $R_L = 1\text{k}\Omega$

$V_{CCA} =$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, V_{CCB} =$				Units
	4.5V to 5.5V	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	
	Min.	Min.	Min.	Min.	
<b>4.5V to 5.5V</b>	40	35	30	20	MHz
<b>3.0V to 3.6V</b>	35	35	30	20	MHz
<b>2.3V to 2.7V</b>	30	30	25	20	MHz
<b>1.65V to 1.95V</b>	20	20	20	20	MHz

#### Notes:

7. Dynamic output characteristics are guaranteed but not tested.
8.  $V_{CCO}$  is the  $V_{CC}$  associated with the output side.
9. See Figure 5.
10. See Figure 6.
11. Maximum data rate is guaranteed but not tested.

### AC Characteristics (Output Load: C<sub>L</sub> = 50pF, R<sub>L</sub> = 1kΩ)

V<sub>CCA</sub> = 4.5V to 5.5V

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, V <sub>CCB</sub> =								Units
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	A to B	1.0	4.5	1.5	5.5	2.0	7.0	3.0	11.5	ns
	B to A	1.0	4.5	1.5	5.5	1.5	6.5	2.5	9.5	
t <sub>PHL</sub>	A to B	2.0	6.0	2.5	6.5	3.0	8.0	4.0	12.5	ns
	B to A	2.0	6.0	2.5	7.0	3.0	8.0	3.5	12.0	
t <sub>PZL</sub>	OE to A		9.5		10.0		11.5		18.0	ns
	OE to B		9.0		11.0		13.5		22.0	
t <sub>PLZ</sub>	OE to A		26.5		26.5		26.5		26.5	ns
	OE to B		26.0		26.5		20.5		15.5	
t <sub>skew</sub> <sup>(12)</sup>	A Port, B Port		0.5		0.5		0.5		0.5	ns

V<sub>CCA</sub> = 3.0V to 3.6V

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, V <sub>CCB</sub> =								Units
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	A to B	1.5	5.5	1.5	6.5	2.0	8.0	3.0	12.0	ns
	B to A	1.5	5.5	1.5	6.5	2.0	7.5	2.5	10.5	
t <sub>PHL</sub>	A to B	2.5	7.0	2.5	7.5	3.0	9.0	4.0	13.0	ns
	B to A	2.5	6.5	2.5	7.5	3.0	9.5	4.0	13.0	
t <sub>PZL</sub>	OE to A		12.5		13.0		15.5		21.0	ns
	OE to B		10.0		12.5		14.5		22.5	
t <sub>PLZ</sub>	OE to A		27.5		28.0		28.0		28.0	ns
	OE to B		27.5		28.0		28.5		22.5	
t <sub>skew</sub> <sup>(12)</sup>	A Port, B Port		0.5		0.5		0.5		0.5	ns

V<sub>CCA</sub> = 2.3V to 2.7V

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, V <sub>CCB</sub> =								Units
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	A to B	1.5	6.5	2.0	7.5	2.5	8.5	3.5	12.5	ns
	B to A	2.0	7.5	2.0	8.0	2.5	8.5	3.0	11.5	
t <sub>PHL</sub>	A to B	3.0	8.5	3.0	9.5	3.0	10.0	4.0	13.5	ns
	B to A	3.0	8.0	3.0	9.0	3.0	10.0	4.5	14.0	
t <sub>PZL</sub>	OE to A		16.0		16.5		18.0		23.5	ns
	OE to B		11.0		14.0		15.5		23.5	
t <sub>PLZ</sub>	OE to A		29.0		29.0		29.5		29.5	ns
	OE to B		29.0		29.0		29.5		29.5	
t <sub>skew</sub> <sup>(12)</sup>	A Port, B Port		0.5		0.5		0.5		0.5	ns

**AC Characteristics** (Continued) (Output Load:  $C_L = 50\text{pF}$ ,  $R_L = 1\text{k}\Omega$ )

$V_{CCA} = 1.65\text{V}$  to  $1.95\text{V}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{CCB} =$								Units
		4.5V to 5.5V		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH}$	A to B	2.5	9.5	2.5	10.5	3.0	11.5	4.0	15.0	ns
	B to A	3.0	11.5	3.0	12.0	3.5	12.5	4.0	15.0	
$t_{PHL}$	A to B	3.5	11.5	4.0	12.5	4.5	14.0	5.0	15.5	ns
	B to A	4.0	12.5	4.0	13.0	4.0	13.5	5.0	15.5	
$t_{PZL}$	OE to A		27.0		27.0		27.0		30.0	ns
	OE to B		18.0		19.5		22.5		29.0	
$t_{PLZ}$	OE to A		34.0		34.0		34.5		35.0	ns
	OE to B		31.5		32.5		33.5		36.5	
$t_{skew}^{(12)}$	A Port, B Port		0.5		0.5		0.5		0.5	ns

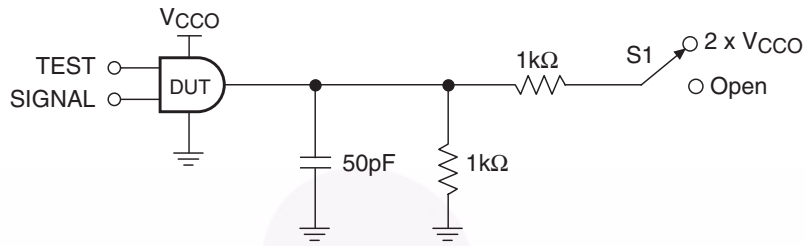
**Note:**

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An or Bn) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW). See Figure 8. Skew is guaranteed but not tested

**Capacitance**

Symbol	Parameter	Conditions	$T_A = +25^\circ\text{C}$	Units
			Typical	
$C_{in}$	Input Capacitance Control pin (OE)	$V_{CCA} = V_{CCB} = \text{GND}$	4	pF
$C_{i/o}$	Input/Output Capacitance, $A_n$ , $B_n$	$V_{CCA} = V_{CCB} = 5.0\text{V}$ , $\text{OE} = V_{CCA}$	6	pF
$C_{pd}$	Power Dissipation Capacitance	$V_{CCA} = V_{CCB} = 5.0\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$ , $f = 10\text{MHz}$	40	pF



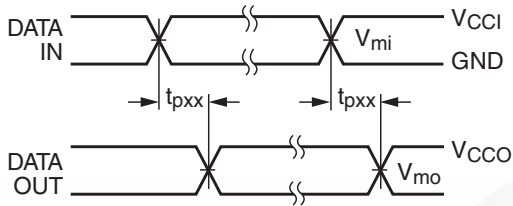


Test	Input Signal	Output Enable Control	S1 Position
$t_{PLH}$ , $t_{PHL}$	Data Pulses	$V_{CCA}$	Open
$t_{PZL}$ (OE to $A_n$ , $B_n$ )	0V	LOW to HIGH Switch	$2 \times V_{CCO}$
$t_{PLZ}$ (OE to $A_n$ , $B_n$ )	0V	HIGH to LOW Switch	$2 \times V_{CCO}$

**AC Load Table**

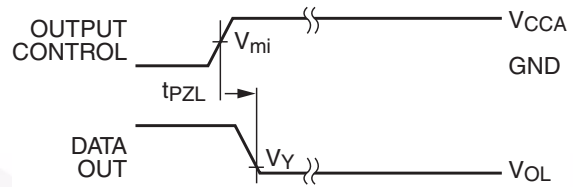
$V_{CCO}$	CI	RI
$1.8V \pm 0.15V$	50pF	1kΩ
$2.5V \pm 0.2V$	50pF	1kΩ
$3.3V \pm 0.3V$	50pF	1kΩ
$5.0V \pm 0.5V$	50pF	1kΩ

Figure 1. AC Test Circuit and AC Load Table



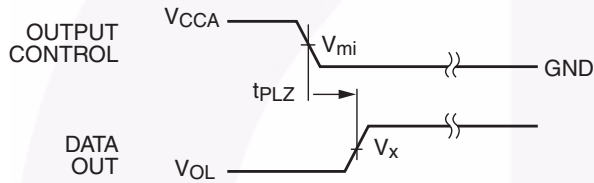
Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% @  $V_I = 1.65\text{V}$  to  $1.95\text{V}$   
 Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% @  $V_I = 2.3$  to  $2.7\text{V}$   
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_I = 3.0\text{V}$  to  $3.6\text{V}$  only  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_I = 4.5\text{V}$  to  $5.5$  only

**Figure 2. Waveform for Inverting and Non-inverting Functions**



Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% @  $V_I = 1.65\text{V}$  to  $1.95\text{V}$   
 Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% @  $V_I = 2.3$  to  $2.7\text{V}$   
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_I = 3.0\text{V}$  to  $3.6\text{V}$  only  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_I = 4.5\text{V}$  to  $5.5$  only

**Figure 3. 3-STATE Output Low Enable Time**



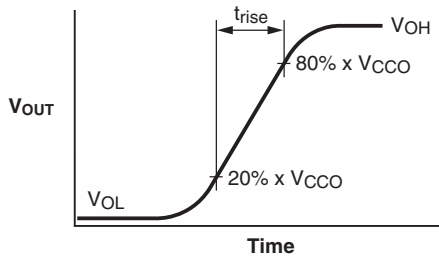
Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% @  $V_I = 1.65\text{V}$  to  $1.95\text{V}$   
 Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90% @  $V_I = 2.3$  to  $2.7\text{V}$   
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_I = 3.0\text{V}$  to  $3.6\text{V}$  only  
 Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_I = 4.5\text{V}$  to  $5.5$  only

**Figure 4. 3-STATE Output High Enable Time**

Symbol	Vcc
$V_{mi}^{(13)}$	$V_{CCI} / 2$
$V_{mo}$	$V_{CCO} / 2$
$V_X$	$0.5 \times V_{CCO}$
$V_Y$	$0.1 \times V_{CCO}$

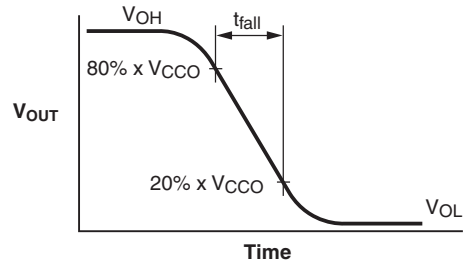
**Note:**

13.  $V_{CCI} = V_{CCA}$  for control pin OE or  $V_{mi} = (V_{CCA} / 2)$ .



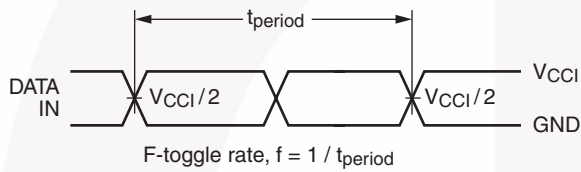
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

**Figure 5. Active Output Rise Time and Dynamic Output Current High**

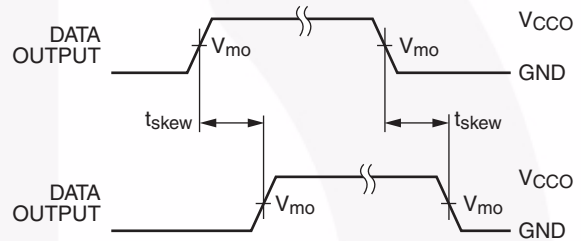


$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

**Figure 6. Active Output Fall Time and Dynamic Output Current Low**



**Figure 7. Maximum Data Rate (or F-toggle) in MHz**



$$t_{skew} = (t_{pHLmax} - t_{pHLmin}) \text{ or } (t_{pLHmax} - t_{pLHmin})$$

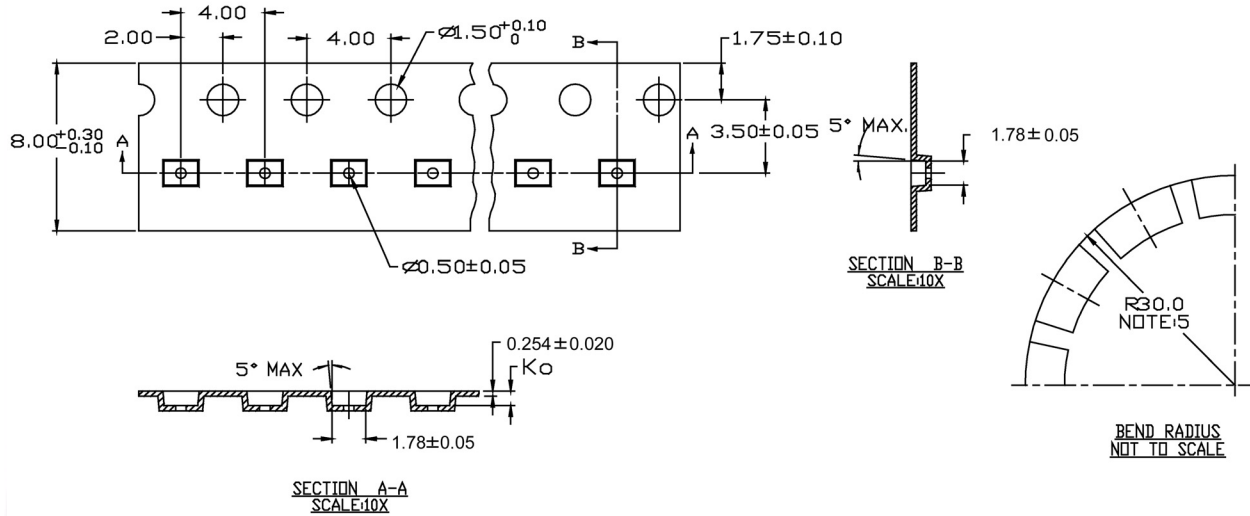
**Figure 8. Output Skew Time**

## Tape and Reel Specification

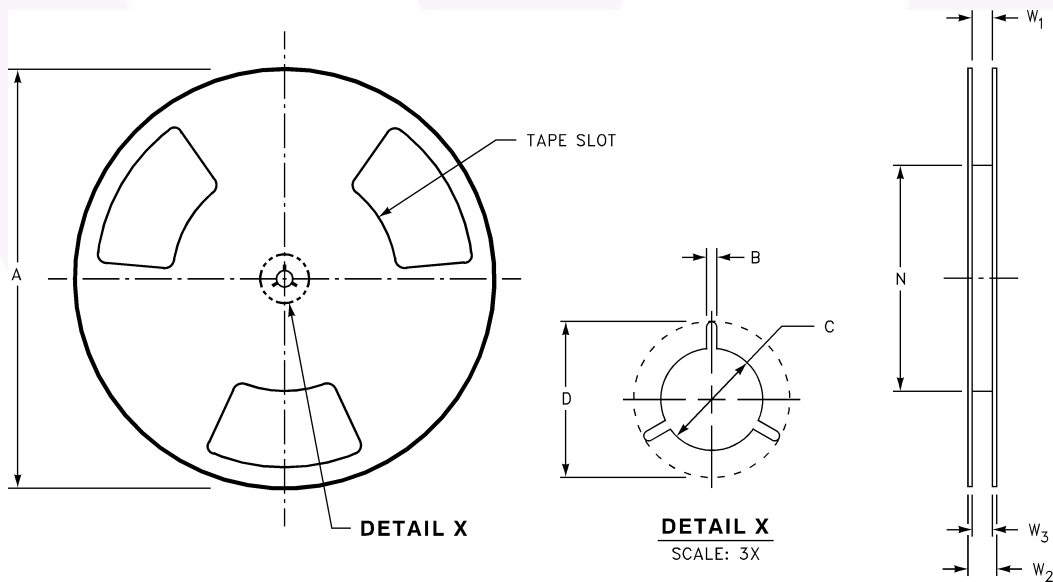
### Tape Format for MicroPak

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

### Tape Dimensions inches (millimeters)

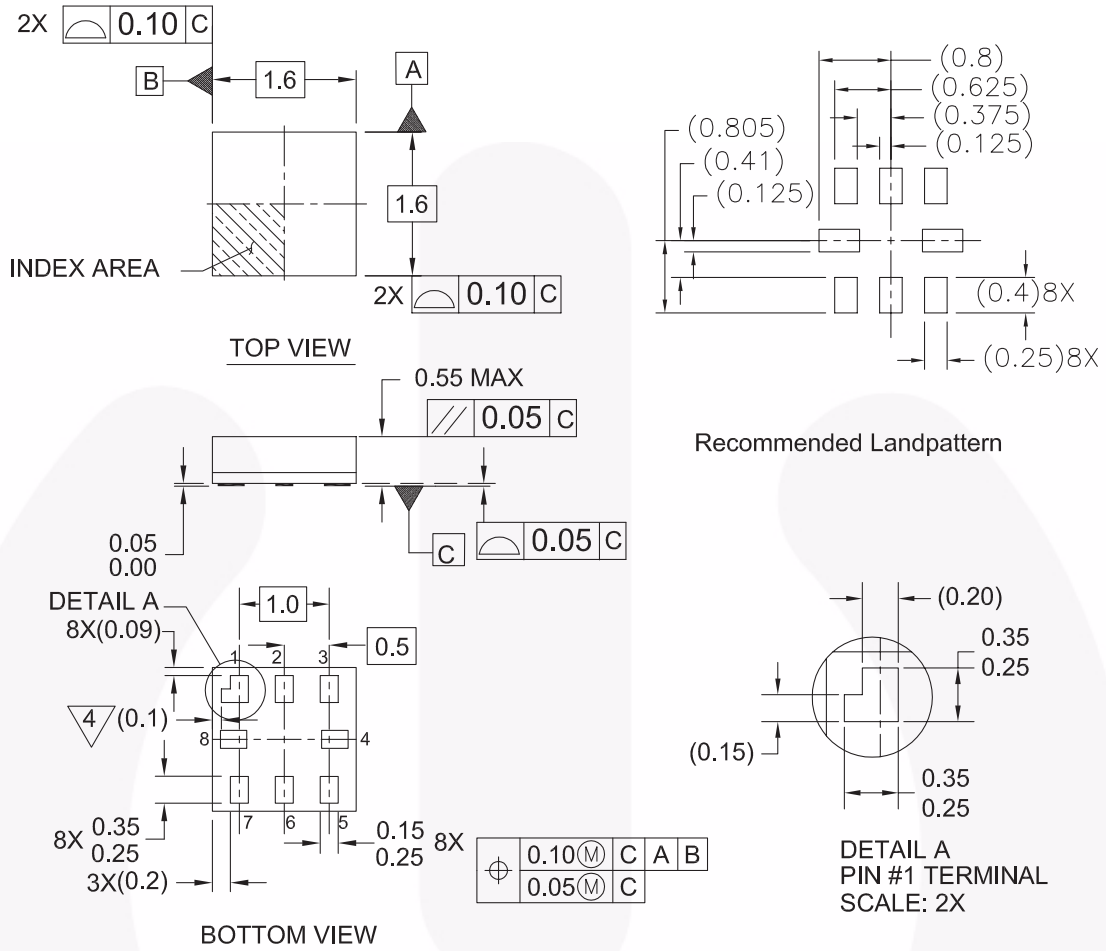


### Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 +0.059/-0.000 (8.40 +1.50/-0.00)	0.567 (14.40)	W1 +0.078/-0.039 (W1 +2.00/-1.00)

## Physical Dimensions



### Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

**Figure 9. 8-Lead MicroPak, 1.6 mm Wide**

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| CorePOWER™  | Global Power Resource™ | Programmable Active Droop™  | TinyBuck™   |
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| EfficientMax™   | ISOPLANAR™             | Saving our world, 1mW at a time™  | TinyWire™   |
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|  ™ | MICROCOUPLER™          | SMART START™  |  |
|  ™ | MicroFET™              | SPM®  | UHC®  |
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| Fairchild Semiconductor®  | MillerDrive™           | SuperFET™   | UniFET™   |
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| FACT®   | Motion-SPM™            | SuperSOT™-6   | VisualMax™  |
| FAST®   | OPTOLOGIC®             | SuperSOT™-8   |   |
| FastvCore™  | OPTOPLANAR®            | SupreMOS™   |   |
| FlashWriter®  |                        | SyncFET™  |   |
|   |                        |  |   |

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