MPC8568E PowerQUICC™ III Processor

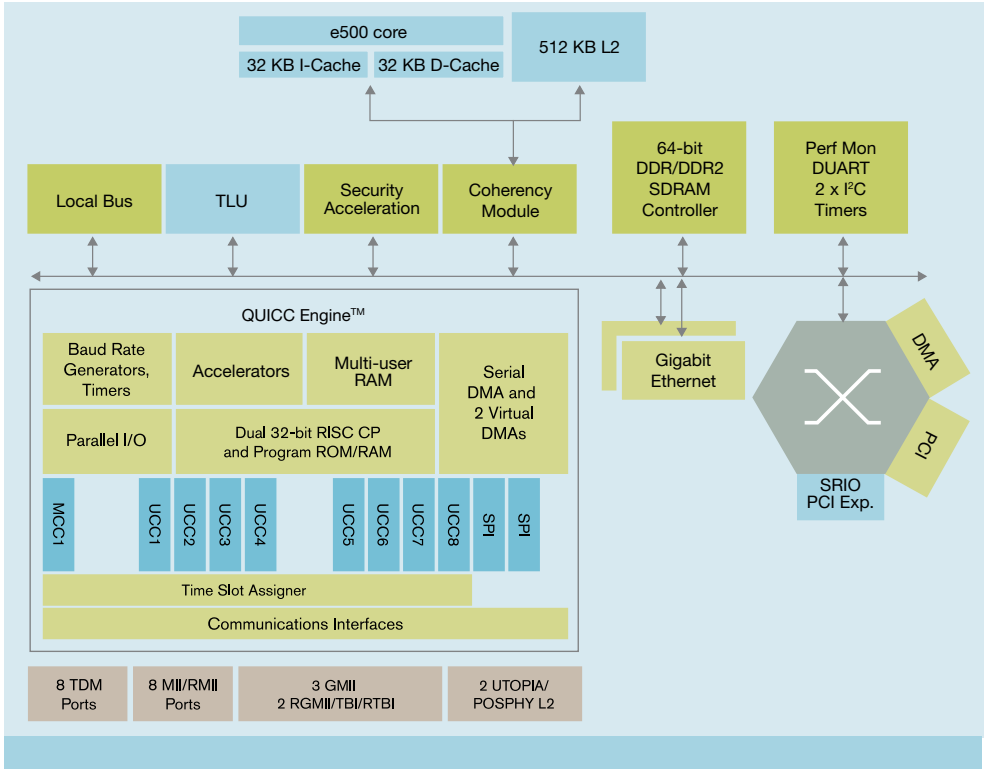
Overview

The MPC8568E PowerQUICC™ III family is designed to address the increasing performance requirements for broadband access equipment including 3G/WiMAX/LTE base stations, RNC's, gateways and ATM/TDM/IP equipment. The MPC8568E enables both IP and multi-protocol solutions, combining a high-performance e500 processor core, built on Power Architecture™ technology, scaling up to 1.33 GHz with a flexible communications engine and high-speed system interfaces, enabling customers to handle many functions in a single chip solution that otherwise would require multiple devices. Ultimately this high level of integration provides savings in cost, power and board space. The MPC8568E provides multi-protocol support for both protocol termination and interworking for a wide range of communication protocols, including ATM, POS, Ethernet, PPP, HDLC and TDM—allowing the flexibility necessary for broadband access devices. Two enhanced Gigabit Ethernet ports, PCI Express® and Serial RapidIO® interconnect technology enables high-speed links to industry-wide switches, field-programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs) and digital signal processors (DSPs). An integrated security engine supports common encryption algorithms, including the Kasumi algorithm needed for 3G wireless security.

MPC8568E Family of Processors

The MPC8568E family consists of the MPC8568E and the MPC8567E. Both are offered in a 1023-pin FC-BGA package for pin compatibility.

MPC8568E Family Block Diagram integrated Control and Data Path for Network Interface Cards



Key Features

- High level of integration and performance, simplifying board design
- Consistent programming model across the PowerQUICC III family of processors
- Flexible system-on-chip (SoC) platform can help improve time to market
- 90 nm silicon-on-insulator (SOI) technology
- Enhanced high-performance e500 core
- 512 KB L2 cache
- High internal processing bandwidth
- Integrated DDR/DDR2 memory controller
- Two integrated Triple Speed Ethernet Controllers (enhanced TSEC)
- Advanced QUICC Engine™ technology supports a wide range of protocols and associated interworking
- TLU provides off-load for table search functions associated with IP forwarding, firewall and Access Control List (ACL) applications
- Flexible high-speed interconnect interfaces
- Serial RapidIO interconnect technology
- PCI Express support
- PCI and local bus interface support
- Integrated security engine

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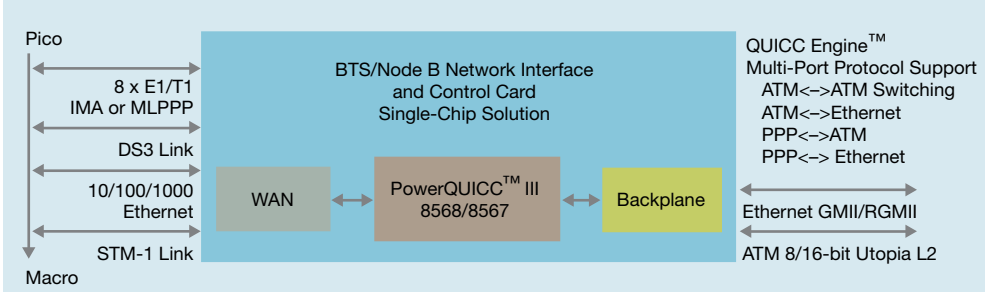
Wireless Node B Network Interface Cards (NIC) Block Diagram



MPC8568E Processor Highlights

	MPC8568E	MPC8567E
Core	e500	e500
CPU Speed	1.0, 1.2, 1.33 GHz	800 MHz, 1.0, 1.2, 1.33 GHz
L1 I/D Cache	32 KB	32 KB
L2 Cache	512 KB	512 KB
Memory Controller	64-bit DDR/DDR2	64-bit DDR/DDR2
Local Bus	32-bit	32-bit
System Interfaces	sRIO, PCI, PCI Express® (x8)	sRIO, PCI, PCI Express (x4)
Stand-Alone 10/100/1000 Ethernet	2 (eTSEC)	-
Table Lookup Unit (TLU)	Yes	No
QUICC Engine™	Up to 533 MHz	Up to 533 MHz
Ethernet	3 x Gigabit, 8 x 10/100	3 x Gigabit, 8 x 10/100
ATM (AAL0,1,2,5)	2 x UTOPIA-L2, 124 M-PHY	2 x UTOPIA-L2, 124 M-PHY
Packet over SONET (POS)	2 x POSPHY-L2, 31 M-PHY	2 x POSPHY-L2, 31 M-PHY
8 TDMs (256 channels of HDLC)	8 x T1/E1, 8 x T3/E3	8 x T1/E1, 8 x T3/E3
Protocol Interworking	Yes	Yes
Security Engine	SEC 2.4	SEC 2.4
Additional Interfaces	DUART, 2 x I²C, 2 x SPI	DUART, 2 x I²C, 2 x SPI
Interrupt Controller	Yes	Yes
Package	1023 FC-BGA	1023 FC-BGA

Technical Specifications

- Embedded e500 core, scaling up to 1.33 GHz
  - 3199 MIPS at 1.33 GHz (estimated Dhrystone 2.1)
  - 36-bit physical addressing
  - Double-precision embedded floating point
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32 KB data and 32 KB instruction
  - L2 cache—512 KB (8-way set associative)
- Integrated DDR memory controller with full ECC support
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4
- Two on-chip, triple-speed Ethernet controllers supporting 10 Mbps, 100 Mbps and 1 Gbps Ethernet/IEEE® 802.3 networks with MII, RMII, GMII, RGMII, RTBI and TBI physical interfaces
- QUICC Engine technology
  - Protocol Support:
    - ATM SAR up to 622 Mbps (OC-12) full duplex
    - PPP, multi-link (ML-PPP), multi-class (MC-PPP) and PPPmux
    - IP termination support for IPv4
    - L2 Ethernet interworking
    - ATM (AAL2/AAL5) to Ethernet (IP) interworking
    - Extensive support for Ethernet RMON/MIB statistics
    - 256 channels of HDLC/Transparent or 128 channels of SS#7
  - Serial Interfaces:
    - Two UL2/POS-PHY interfaces
    - Three 1 Gbps Ethernet interfaces using GMII. Two 1 Gbps Ethernet interfaces using RGMII, TBI and RTBI
    - Up to eight 10/100 Mbps Ethernet interfaces using MII or RMII
    - Up to eight T1/E1/J1 interfaces or eight T3/E3 interfaces
    - Dual SPI interfaces
- Serial RapidIO and PCI Express high-speed interconnect interfaces
- Table lookup unit
- On-chip network (OCeaN) switch fabric
- 32-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
- 166 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Dual I²C and Dual Universal Asynchronous Receiver/Transmitter (DUART) support
- Programmable interrupt controller (PIC)
- IEEE 1149.1 JTAG test access port
- 1.1V core voltage with 3.3V, 2.5V and 1.8V I/O
- 1023-pin FC-BGA package

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

Document Number: MPC8568FS
REV 2

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